REMARKS

Claims 1 - 8, 12, 14 - 34 and 36 are pending in the present application, of which claims 15 - 34 have been withdrawn from consideration. By this Amendment, claims 2 and 36 have been amended. No new matter has been added. It is believed that this amendment is fully responsive to the Office Action dated October 15, 2003.

Allowable Subject Matter:

Applicant gratefully acknowledges the Examiner's indication on page 6 in the outstanding Office Action that claims 1, 4, 12 and 14 are allowable.

35 U.S.C. §112 First Paragraph Rejection

Claims 2, 3 and 5 – 8 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

This rejection is respectfully traversed.

It is respectfully submitted that claim 2 has been amended to overcome this rejection. Accordingly, withdrawal of this rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hosotani, et al. (USP 5,977,583) in view of Kimura (USP 6,127,734). Claims 5 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hosotani et al. in view of Kimura and Fukase (USP 5,728,596).

Each of these rejections is respectfully traversed.

The Examiner states that in configuration of an inter-layer insulation film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration, so that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Hosotani et al. by forming the first inter-layer insulation film on the side walls of the conductor patters as taught by Kimura to simplify the manufacturing process and increase the degree of integration. In the Response to Argument, the Examiner states that the sidewall spacers 21 of Hosotani et al. are not necessary between the adjacent conductors where the insulating layer 22 is formed, and there is no need for protection because there is no conductive material between the adjacent conductors.

However, in Hosotani et al., in regions where the contact holes are formed, the sidewall spacers 21 are formed in order to insulate the plug 25 from the gate electrode, so that the sidewall spacers 21 formed at least in these regions are essential. Thus, in

Hosotani et al., the sidewall spacers 21 must be formed. In order to fabricate the structure having no sidewall spacers 21 between the adjacent conductors where the insulating layer 22 is formed, it is necessary to selectively remove the sidewall spacers 21. However, such steps bring about no technical advantages. On the contrary, the manufacturing steps are increased, and the damages are introduced into the ground structure during the removal of the sidewall spacers. Thus, one of ordinary skill in the art would not remove the sidewall spacers 21 between the adjacent conductors where the insulating layer 22 is formed.

In Response to Arguments, the Examiner states that if one were to increase the degree of integration or reduce manufacturing steps, one of ordinary skill in the art would not form the spacers on the side of the conductor where there is no contact hole formed, as explained in Kimura. However, this is not correct. As described in column 19, lines 13-16, Kimura has not excluded the transistors having LDD structure, *i.e.,* the transistors having sidewall spacers. It means that the invention of Kimura does not relate to the presence or absence of the sidewall spacers. The Examiner recognizes that the absence of the sidewall spacers contributes to downsizing of the semiconductor devices. However, the presence or absence of the sidewall spacers is independent of downsizing of the semiconductor devices. In the present invention, according to the presence of the sidewall insulation film, downsized contact holes can be formed with the simplified manufacturing steps.

Thus, Hosotani et al. and Kimura are clearly different from the present invention and do not provide any motivation for the present invention.

Claim 36:

Claim 36 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fukase in view of Kimura.

This rejection is respectfully traversed.

The Examiner states that in configuration of an inter-layer insulation film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration, so that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Fukase by forming the first inter-layer insulation film on the side walls of the conductor patterns as taught by Kimura to simplify the manufacturing process and increase the degree of integration. In the Response to Arguments, the Examiner states that a spacer is not particularly needed for the middle conductor pattern 4a in FIG. 2G because there are no LDD regions next to the gate, therefore application of spacers for that conductor pattern is a non critical step.

However, in Fukase, from the viewpoint of improving both of the characteristics of the peripheral transistor and the contact characteristics in the memory cell region, after the sidewall insulation film 10 optimized based on the characteristics of the peripheral

transistor is removed, the sidewall insulation film 17 is again formed in the contact hole in the memory cell region (*see* FIGS. 2A-2G of Fukase). That is, Fukase has applied such the process on the assumption that the peripheral transistor having the LDD structure is formed. It is contrary to the premise of Fukase not to form the sidewall insulation film 10 on the side walls of the conductor patterns.

Additionally, as described above, the invention of Kimura does not relate to the presence or absence of the sidewall spacers. Absence of the sidewall spacers does not contribute to downsizing of the semiconductor devices, etc. Thus, one of ordinary skill in the art would not remove the sidewall insulation film of Fukase, even though Kimura shows a semiconductor device having the inter-layer insulation film 11 formed on the substrate in contact with the side walls of the conductor patterns.

Thus, Fukase et al. and Kimura are clearly different from the present invention and do not provide any motivation for the present invention.

For at least the foregoing reasons, it is believed that this application is now in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is believed that this application is not in condition for allowance, the Examiner is encouraged to contact the Applicant's undersigned attorney at the telephone number below to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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